

REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-9 remain pending in the application. Claims 7-9 have been allowed. By the foregoing amendment, claims 5 and 6 have been amended. However, the amendments to claims 5 and 6 are not considered to raise a new issue, as the feature added has been considered with respect to independent claim 1.

In numbered paragraph 4 of the Office Action, Claims 1-4 are rejected based on a new ground of rejection under 35 U.S.C. §103. These claims are rejected as being unpatentable over U.S. Patent No. 6,079,030 (Masubuchi) in view of what is asserted to be Applicant's admitted prior art (AAPA) and newly cited U.S. Patent No. 6,292,880 (Mattis et al). On page 5 of the Office Action, claims 5-6 are rejected under 35 U.S.C. §103 as being unpatentable under the Masubuchi patent in combination with the alleged AAPA. These rejections are respectfully traversed.

Exemplary embodiments of the present invention are directed to a fault tolerant computer system, having an application memory, such as the application memory 21 of main memory 20 in Applicant's exemplary Fig. 3 embodiment, organized as a plurality of cache lines. Each cache line is identified by an address in the memory. A CPU, such as processor 31 or 32, is provided for executing instructions stored in the application memory. A state memory, such as status buffer 25, is provided for storing contents of internal registers of the CPU. In the Figure 3 embodiment, a check point controller 43

defines a series of repeating checkpoint cycles. A memory controller 41 of the Fig. 3 embodiment operates the application memory 21 and a FIFO buffer 22.

In operation, the memory controller 41 receives a cache line from the CPU in response to a write command specifying an address in the application memory 21 at which the cache line is to be stored. A copy of the cache line as stored in the application memory is copied into the FIFO buffer 22 upon receiving a first write command after the start of the current checkpoint cycle, but not on a subsequent write command during the current checkpoint cycle.

In accordance with exemplary embodiments, a copy of a cache line is only stored the first time that the cache line is written during a current checkpoint cycle. As such, a much smaller buffer memory can be used, since copies of the cache line are not stored on subsequent writes to the same address of the buffer during the current checkpoint cycle.

The foregoing features are broadly encompassed by Applicant's claim 1 combination which is directed to a computer comprising, among other features, application memory, a FIFO buffer, a CPU, a state memory, a checkpoint controller and a memory controller. The memory controller receives a cache line from the CPU in response to a write command specifying an address A in said application memory at which said cache line is to be stored, wherein a copy of said cache line is stored in said application memory at address A, is copied into said FIFO buffer upon receiving first write command specifying A after the start of the current checkpoint cycle, but not on a subsequent write command specifying A during said current checkpoint cycle.

Such features are neither taught nor suggested by the Masubuchi patent, considered alone or in combination with what the Examiner alleges to be AAPA and/or the Mattis patent.

The Masubuchi patent is directed to a memory state recovering apparatus similar to that described in the background portion of Applicants' specification. This patent describes a system which stores contents of a cache line in a buffer, such as "Before Image Buffer" 28 of Fig. 10 in the Masubuchi patent, with the address of the cache line. In contrast to the exemplary embodiments of the present invention, an entry is made in the buffer each time a cache line is overwritten, regardless of whether a previous copy of that cache line already exists in the buffer. As such, the Masubuchi patent specifically teaches away from exemplary embodiments of the present invention, as this patent fails to teach or suggest optimizing error recovery in a fault-tolerant computer system. In addition, the patent provides no teaching or suggestion for using a FIFO buffer as an efficient buffer for storing plural cache lines as presently claimed.

The Examiner asserts that AAPA discloses a FIFO buffer. However, Applicants' background section of the present application neither teaches nor suggests using a FIFO buffer configured in conjunction with the memory controller to receive a first write command specifying an address A after the start of the current checkpoint cycle, but not on a subsequent write command specifying A during said current checkpoint cycle.

In rejecting claim 1, the Examiner relies on the newly cited Mattis patent and asserts in the last paragraph on page 3 of the Office Action that:

Furthermore, Mattis discloses storing only one copy of data in cache (see abstract), indicating receiving the first write command specifying A after the start of the current checkpoint cycle, but not on a subsequent write command specifying A during said current checkpoint cycle.

However, Mattis documents disclose any use of a checkpoint cycle. Despite this, The Examiner concludes in the first paragraph on page 4 of the Office Action that:

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to receive first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle. A person of ordinary skill in the art would have been motivated to make the modification to Masubuchi because storing only one copy enables the storage usage to be dramatically reduced, as per teaching of Mattis (see abstract).

Contrary to the Examiner's assertion, the Mattis patent does not teach or suggest configuring a cache as a FIFO buffer which receives a first write command specifying an address A after a start of a current checkpoint cycle, but not on a subsequent write command specifying A during said current checkpoint cycle. In addition, there would have been no suggestion or motivation to have used features of the Mattis patent in conjunction with the Masubuchi patent.

The Mattis patent is directed to an alias-free content-indexed object cache, and is not directed to a checkpoint error recovery system to recover from system failures. The Mattis patent abstract describes caching information objects stored in portions of a non-volatile storage device called arenas. Objects are allocated within an arena and are mapped to directory tables that provide an efficient search mechanism. The name key and the

content key are constructed using a hash function. Directory tables are provided to store tags and subkeys derived from the keys. Duplicate objects having different names will hash to the same content key. The cache can detect duplicate objects even though they have different names, and store only one copy of the object.

Thus, the Mattis patent is directed to a system which uses directory tables and keys to determine whether multiple object names hash to the same content keys. The Mattis patent therefore fails to overcome the deficiencies described above with respect to the Masubuchi patent and with respect to what the Examiner asserts to be AAPA. None of the documents or disclosures relied upon by the Examiner teach or suggest copying a cache line into a FIFO buffer upon receiving a first write command specifying an address A after the start of the checkpoint cycle, but not on a subsequent write command specifying A during the current checkpoint cycle, the cache line received in the write command replacing the contents of A in the application memory. At best, any combination of the disclosures relied upon by the Examiner would have resulted in storing information objects in the CPU system of the Masubuchi patent using the directory tables and hash functions as described in the Mattis patent without regard to any checkpoint cycles. Moreover, there would have been no teaching or suggestion for using the information object cache method of the Mattis patent in the memory state recovering apparatus of the Masubuchi patent, or of using a FIFO memory as the cache memory in the Masubuchi patent.

As such, claim 1 is allowable over the documents and disclosure relied upon by the Examiner. Independent claims 5 and 6 recite features similar to those discussed above and are therefore also allowable over the documents relied upon by the Examiner.

Claim 5 is directed to a computer system comprising, among other features, as application memory, a FIFO buffer, a CPU, a state memory, a checkpoint controller and a memory controller. The memory controller is provided for operating said application memory and said FIFO buffer, said memory controller receiving a cache line from said CPU in response to a write command specifying an address A in said application memory at which said cache line is to be stored. A copy of said cache line as stored in said application memory at address A, is copied into said FIFO buffer upon receiving the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle. The checkpoint controller causes said computer system to be reconfigured before restarting said computer system.

On page 6 of the Office Action, the Examiner acknowledges that the Masubuchi patent fails to disclose a FIFO buffer wherein said checkpoint controller causes said computer system to be reconfigured before restarting said computer system. In the last paragraph on page 6 of the Office Action, the Examiner takes official notice as follows:

Official Notice is taken wherein said checkpoint controller causing said computer system to be reconfigured before starting said computer system. It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the teaching of Masubuchi to have said checkpoint controller causing said computer system to be

reconfigured before restarting the computer system because applicant clearly states that it would have been obvious to do so, stating that machines could be reconfigured prior to restart (see pg. 9, lines 12-17 of applicants' disclosure)

These assertions are respectfully traversed. Applicant asserts on specification page 9, lines 7-11 that a computer system, configured with a checkpoint controller having characteristics as described in Applicant's detailed description, can be reconfigured prior to restart. Applicants' request that the Examiner provide some teaching in the prior art which forms the basis for the assertion of Official Notice other than Applicant's own description of exemplary embodiments of the present invention. In the absence of providing any such teaching, Applicants' request withdrawal of this rejection and allowance of claim 5.

Regarding claim 6, the Examiner asserts on page 8 of the Office Action that:

It would have been obvious to one of ordinary skill at the time the invention was made to modify the teaching of Masubuchi to use a FIFO buffer. A person of ordinary skill in the art would have been motivated to make the modification to Masubuchi because Masubuchi disclose a buffer for retaining the preceding state of the memory and a FIFO buffer, as per teaching of AAPA, constitutes a buffer, which can be used to retain a preceding state of memory.

Contrary to the Examiner's assertions, the Masubuchi patent, considered individually or in combination with what the Examiner asserts to be AAPA, fails to teach or suggest the computer system as recited in Applicants' claim 6. For example, the Masubuchi patent is not directed to computer system which comprises, among other features, an application memory, a FIFO buffer, a CPU, a state memory, a checkpoint

controller, and a memory controller, wherein said application memory comprises a fault tolerant memory. As described on specification page 6 of Applicants' application, if a fault is detected, the contents of the exemplary FIFO 22 are written back into application memory 21 during a fault recovery phase to return the application memory to the state it had at the end of the last checkpoint cycle. In addition claim 6 has been amended to recite that a copy of said cache line as stored in said application memory at address A, is copied into said FIFO buffer upon receiving a first write command specifying A after the start of the current checkpoint cycle, but not on a subsequent write command specifying A during said current checkpoint cycle.

For reasons already discussed with respect to claim 1, claim 6 is considered allowable over the documents relied upon by the Examiner.

In light of the foregoing, all of Applicants' independent claims are considered allowable, and a Notice of Allowance is respectfully solicited.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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By: _____



Patrick C. Keane

Registration No. 32,858

Hewlett Packard Company
Intellectual Property Administration
P.O. Box 272400
Ft. Collins, CO 80527-2400
(703) 848-6522